The New Generation of Phytium’s 64 Cores Processor and its Ecosystem

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Phytium Technology Co., Ltd
Chip development —— Highend Processor MarsII

• 16nm
• 2.3GHz
• 64 cores (FTC-662), ARM V8 compatible
• Peak performance 588.8GFlops
• 8*DDR4-2400 memory access channel, peak memory bandwidth 153.6GB/s
• 33 * lane PCIe 3.0 interface
Chip development —— Highend Processor MarsII

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Chip development —— Highend Processor MarsII

- Fab process: 16nm FF+ GL 1P11M+RDL
- Frequency: 2.3GHz
- TPD: 96W
- Die size: 370mm^2
- Design scale: 6 billion transistors
Chip development —— Highend Processor MarsII

- Package size: 61mm x 61mm
- Package type: FCBGA
- Bumps: 11916
- Balls: 3576
### China Electronics Standardization Institute CESI lab Test results

<table>
<thead>
<tr>
<th>Test item</th>
<th>Test result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td><a href="mailto:2.3GHz@0.9V">2.3GHz@0.9V</a></td>
</tr>
<tr>
<td>Dual precision floating peak performance</td>
<td>588.776GFlops</td>
</tr>
<tr>
<td>Single chip LINPACK</td>
<td>510.81GFlops</td>
</tr>
<tr>
<td>Single chip LINPACK efficiency</td>
<td>86.75%</td>
</tr>
<tr>
<td>Chip energy-efficiency</td>
<td>6.13GFlops/W</td>
</tr>
<tr>
<td>SPEC CPU 2006</td>
<td></td>
</tr>
<tr>
<td>integer</td>
<td>510</td>
</tr>
<tr>
<td>float</td>
<td>470</td>
</tr>
<tr>
<td>STREAM bandwidth</td>
<td>89GB/s</td>
</tr>
</tbody>
</table>
### Chip development —— Compare with Intel products

<table>
<thead>
<tr>
<th></th>
<th>SPEC 2006 Chip integer performance</th>
<th>SPEC 2006 Chip float performance</th>
<th>TPD</th>
</tr>
</thead>
<tbody>
<tr>
<td>IntelXeonX5670 (6 cores, 2.93G, 2010)</td>
<td>171</td>
<td>121</td>
<td>95W</td>
</tr>
<tr>
<td>IntelXeonE5-2692v2 (12 cores, 2.2G, 2013)</td>
<td>456</td>
<td>329</td>
<td>115W</td>
</tr>
<tr>
<td>IntelXeonE5-2695v3 (14 cores, 2.3G, 2014)</td>
<td>557</td>
<td>410</td>
<td>120W</td>
</tr>
<tr>
<td>IntelXeonE5-2699v3 (18 cores, 2.3G, 2015)</td>
<td>693</td>
<td>460</td>
<td>145W</td>
</tr>
<tr>
<td>IntelXeonE5-2699v4 (22 cores, 2.2G, 2016)</td>
<td>837</td>
<td>533</td>
<td>145W</td>
</tr>
<tr>
<td>IntelXeonE7-8890v4 (24 cores, 2.2G, 2017)</td>
<td>880</td>
<td>590</td>
<td>165W</td>
</tr>
<tr>
<td>MarsII, 64 core 2.3GHz (2017)</td>
<td>508</td>
<td>470</td>
<td>96W</td>
</tr>
</tbody>
</table>
Key technology breakthrough —— Challenges

- **Multi-core general-purpose micro processor challenges**
  - General-purpose micro processor has high requirement for the balance between calculation and memory access
  - Accompanying with cores increasing, chip size and large network scale bring problems
    - Internal cores data exchange, memory access has larger delay
    - Aggravate memory wall problem
    - Huge challenges for physical design, full chip top level timing convergence becomes more and more difficult
Key technology breakthrough —— points

- Data affinity multi-core CPU architecture
- High energy-efficient disorder superscalar CPU cores
- Hierarchical on-chip parallel storage architecture
- Hierarchical heterogeneous on-chip network
- 16nm high performance low-power high-density CPU physical design
- Large-size low-power package technique
Key technology breakthrough —— Data affinity multi-core CPU architecture

• **Data affinity multi-core CPU architecture**
  - Fully used application locality characters, give support for locality in architecture level
    - Whole chip are divided into several levels, each level owns independent calculation, memory access, IO resources
      - Higher level has more resources but slower, while lower level has fewer resources but faster
    - Software uses the affinity scheduling mechanism to limit application and data as low level as possible to increase performance and energy efficient

• **Advantages**
  - Using locality remits memory wall problem in multi-core CPU
  - Hierarchical design, easy to extend to larger design with more cores
  - Simplify physical design
Key technology breakthrough —— Data affinity multi-core CPU architecture

- MarsII 64 cores, divided into 8 Panels
- Each Panel has independent calculation, memory resources
  - 8 cores
  - 4MB L2 Cache
  - 1 DDR4 memory control unit
  - 1 NoC router unit
Key technology breakthrough —— High energy-efficient disorder superscalar CPU core

- **4 launching disorders based superscalar CPU core**

- **FTC-662**

  - Fetch instruction
    - 32KB level1 instruction Cache
    - Multi-stage hybrid branch predictor

  - Decode:
    - 4 instructions/cycle

  - Dispatch: order
    - 4 instructions/cycle

  - Execute: disorder
    - 4 integer unit, 2 floating unit
    - 2 memory access pipelines
    - 32KB level1 data Cache
Key technology breakthrough —— High energy-efficient disorder superscalar CPU core

- Multi-level Hybrid branch predictor
  - Static branch predict
  - Multi-length history information predict
  - Indirect predict
  - Return address stack
  - Loop detector
- Based on confidence coefficient determine best branch
- Branch predict failure rate less than 2%
Key technology breakthrough — High energy-efficient disorder superscalar CPU core

- **Low delay calculation unit**
  - Float multiplication 3 cycles
  - Float addition 3 cycles
  - Longest Float division 16 cycles
- **Support floating data format**
  - 32bit single precision
  - 64bit double precision
  - 2-path SIMD
Key technology breakthrough —— High energy-efficient disorder superscalar CPU core

- **Balanced dispatch scheduling strategy**
  - Each cycle decode 4 instructions
  - Use 8-depth dispatch queue
    - Order dispatch
    - Based on queue free status dispatch
  - Balance registers queues
    - 192 result queues
  - Registers ports share
    - Each cycle need 16 read ports at the most
    - Reduce 4 ports by sharing ports optimization
Key technology breakthrough —— Hierarchical heterogeneous on-chip network

- **Hierarchical heterogeneous hybrid exchange network**
  - Local interconnect coupling cores and L2 cache as cluster, the data in cluster has strong locality, short communication distance and small delay
  - Global interconnect can be implemented by a configurable cell-network to connect each cluster to gain better system expansibility and flexibility
Key technology breakthrough —— Hierarchical heterogeneous on-chip network

- **Low-delay high-throughput rate communication cell**
  - First-come-first-served, fair rotation arbitration strategy
  - Low delay (3 cycles/hop)
  - High bandwidth (64 GBps/port)
  - 5 individual physical channels
  - Ports amount can be configured for device connection or cascading
Key technology breakthrough —— Energy-efficiency

- Consume power by demand, power adjust proportional to load
  - Measured energy-efficiency 6.13GFlops/W

<table>
<thead>
<tr>
<th></th>
<th>Peak performance (Gflops)</th>
<th>Power (W)</th>
<th>Peak energy-efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>MarsII</td>
<td>588.8</td>
<td>96</td>
<td>6.13</td>
</tr>
<tr>
<td>Xeon 1650v3</td>
<td>211.2</td>
<td>110</td>
<td>1.92</td>
</tr>
<tr>
<td>Xeon 2695v3</td>
<td>515.2</td>
<td>120</td>
<td>4.29</td>
</tr>
<tr>
<td>Xeon 2699v4</td>
<td>774.4</td>
<td>145</td>
<td>5.35</td>
</tr>
</tbody>
</table>
Ecosystem

Base Ecosystem + System Ecosystem + Application Ecosystem

arm

Linaro

SAP

Office System

ERP

OA

Middleware

DATABASE

OS

CLOUD

DATABASE
Fusion OS

- Linux application
- Android APP
### Storage

<table>
<thead>
<tr>
<th></th>
<th>ACS 5000A</th>
<th>MS3000G2-FT</th>
<th>X86 Based</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOPS</td>
<td>Sequence Read</td>
<td>821059</td>
<td>721002</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>Sequence Read</td>
<td>8404</td>
<td>6400</td>
</tr>
</tbody>
</table>

![Storage Diagram]

- **FC**
- **IB**
- **NIC**
- **NTB**
- **Mars2**
- **PCIe Switch**
- **Midplane**
- **NVMe SSD**

**Phytium Technology Co., Ltd.**
### Database

<table>
<thead>
<tr>
<th>Server</th>
<th>Core number</th>
<th>Theoretical performance Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel Xeon E5-2699 <a href="mailto:v3@2.3GHz">v3@2.3GHz</a>, Dual</td>
<td>36</td>
<td>Whole Chip: 2.5X; Single Thread: 3X;</td>
</tr>
<tr>
<td>Mars2@, Single</td>
<td>64</td>
<td></td>
</tr>
</tbody>
</table>

- **Results**
  - 8a: OLAP chip 1.3X~1.6X; single thread 2.1X~2.6X;
  - 8t: OLTP 2.3X~2.7X
  - Performance linear growth with threads

- **Conclusion**
  - Accompanying with the increasement of CPU nodes, PHYTIUM server can get almost the same performance as X86 server
EDA TOOLS

- Empyrean sign-off tool: Skipper
- Comparison:
  - PHYTIUM Server, **Earth** CPU 16core 1.5GHz , Memory32G, Kylinx OS4.4.58
  - Intel Xeon (R) CPU 64Core 2.6GHz , Memory 256G , Redhat Enterprise 2.6.32
- Input: hierarchical GDS, file size 6.84G, 79 layer

<table>
<thead>
<tr>
<th></th>
<th>PHYTIUM SERVER</th>
<th>XEON SERVER</th>
</tr>
</thead>
<tbody>
<tr>
<td>Load Data</td>
<td>8.7 s</td>
<td>7.73 s</td>
</tr>
<tr>
<td>Flush GDS</td>
<td>No delay</td>
<td>No delay</td>
</tr>
<tr>
<td>Inquire instance</td>
<td>&lt;1s</td>
<td>&lt;1s</td>
</tr>
</tbody>
</table>
Esports - WEC2018

• WEC2018: Women’s Esports Championship 2018
• 2018.12.14~2018.12.16 (Chengdu, China)
Thank you for your attention!

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