Ongoing research in Bristol: New Drugs ‘In Silico’

- Parkinson’s & Osteoporosis
Multiphysics Simulations: Fluid Dynamics, Heat Diffusion, Electromagnetics

Gas turbine: suck, squeeze, bang, blow
What is “Super” or “High Performance” Computing?

Lake Tahoe ~40 Trillion Gallons of water (4.0x10^12)
~2002 Supercomputers hit 40 Teraflops (Earth Simulator – Japan/NEC)
What is “Super” or “High Performance” Computing?

The Great Lakes hold ~6.5 Quadrillion gallons of water ($6.5 \times 10^{15}$)
2008 Supercomputers hit 1 Petaflop ($1.0 \times 10^{15}$) (US IBM Roadrunner)
Top500 systems over the past 25 years
These are not embedded devices:
Early Research into the Efficacy of Arm for HPC
**Catalyst UK: Accelerating ARM Adoption in UK**

### Program Goals

- **Deployment**: Deployment of HPC clusters at multiple UK sites, supported for 3-year period providing access to academia & industry
- **Adoption**: Early adoption of ARM for HPC in UK; Apollo 70 Early Ship followed by customer collab.
- **Applications**: Customer-driven porting and opt
- **Collaboration**: Leveraging the success "Project Comanche" model of customer-centric collaboration, but based instead on Early Ship HPE Apollo 70 product
- **Exascale**: Establish foundation for Exascale collab

### Industry Partners

- **HPE**: Apollo 70, HPE Performance Software - Cluster Manager, HPE Performance Software – Message Passing Interface
- **ARM**: Adata Studio (Compiler, Libraries, Forge-DDT & MAP), OpenHPC
- **Mellanox**: OFED, HPC-X, OpenMPI, OpenSHMEM, MXM, SHARP
- **SuSE**: SLEs, OpenStack, HPC Module
- **Cavium**: ThunderX2 SoC, technical support
- **Qualcomm**: Centriq SoC, technical support (tentative)

### UK Collaborations

- **EPCC**: WRF, OpenFOAM, Rolls Royce Hydra opt, 2 PhD candidates
- **Leicester**: Data-intensive apps, genomics, MOAB Torque, DIRAC collab.
- **Bristol**: VASP, CASTER, Gromacs, CP2K, Unified Model, Hydra, NAMD, Oasis, NEMO, OpenIFS, CASINO, LAMMPS
- **UK Government**: Dept. for Bus., Energy & Industrial Strategy (BEIS)

### Configs & Timeline

**Typical for each site:**

- 64 Apollo 70
  - Compute Nodes: 2 Cavium 32c, 2.2 GHz
  - 256GB memory (16GB DIMM)
  - 8 EDR CX5 Cloos
  - 4096+ cores
  - 6 CL4300 (tentative)
  - Services/Storage
  - Qualcomm Centriq

**Sep-Dec**: Structure partnership, alignment

**Jan**: HPE/ARM SOW

**Feb**: Customer SoWs, quotations, POs

**Mar**: SW stack validation (3rd Party Runtime library)

**Apr**: Systems build, public announcements

**May**: Delivery and acceptance

### Measures of Success

**Intended outcomes include:**

- Critical HPC apps ported and demonstrated
- ISV engagements and demonstrations
- Demonstrated performance improvements
- Publications and follow-on collaborations
- Bugs filed, fixed & up-streamed to open source

**HPE will deliver >12,000 cores across 3 sites, amongst the largest ARM HPC deployments in the world**

---

*HPE Confidential*
Isambard The World’s First Arm-based Production Supercomputer
Vanguard Astra by HPE: #156 on top500

- 2,592 HPE Apollo 70 compute nodes
  - 5,184 CPUs, 145,152 cores, 2.3 PFLOPs (peak)
- Marvell ThunderX2 ARM SoC, 28 core, 2.0 GHz
- Memory per node: 128 GB (16 x 8 GB DR DIMMs)
  - Aggregate capacity: 332 TB, 885 TB/s (peak)
- Mellanox IB EDR, ConnectX-5
  - 112 36-port edges, 3 648-port spine switches
- Red Hat RHEL for Arm
- HPE Apollo 4520 All-flash Lustre storage
  - Storage Capacity: 403 TB (usable)
  - Storage Bandwidth: 244 GB/s
Exascale – the race underway at the high end

### Projected Exascale System Dates

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<td><strong>U.S.</strong></td>
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<td><strong>EU</strong></td>
<td>PEAK ES: 2023-2024</td>
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<td>Pre-ES: 2020-2022 (~$125M)</td>
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<td>Vendors: US and then European</td>
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<td>Processors: x86, ARM &amp; RISC-V</td>
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<td>Initiatives: EuroHPC, EPI, ETP4HPC, JU</td>
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<td>Cost: Over $300M per system, plus heavy R&amp;D investments</td>
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<td><strong>China</strong></td>
<td>Sustained ES*: 2021-2022</td>
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<td>Peak ES: 2020</td>
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<td>Vendors: Chinese (multiple sites)</td>
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<td>Processors: Chinese (plus U.S.?</td>
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<td>13th 5-Year Plan</td>
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<td>Cost: $350-$500M per system, plus heavy R&amp;D</td>
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<td><strong>Japan</strong></td>
<td>Sustained ES*: ~2021/2022</td>
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<td>Peak ES: Likely as a AI/ML/DL system</td>
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<td>Vendors: Japanese</td>
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<td>Processors: Japanese ARM</td>
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<td>Cost: ~$1B, this includes both 1 system and the R&amp;D costs</td>
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<td>They will also do many smaller size systems</td>
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*1 exaflops on a 64-bit real application

© Hyperion Research
1. High-Performance Arm CPU A64FX in HPC and AI Areas

**Architecture features**

- **ISA**: Armv8.2-A (AArch64 only) SVE (Scalable Vector Extension)
- **SIMD width**: 512-bit
- **Precision**: FP64/32/16, INT64/32/16/8
- **Cores**: 48 computing cores + 4 assistant cores (4 CMGs)
- **Memory**: HBM2: Peak B/W 1,024 GB/s
- **Interconnect**: TofuD: 2B Gbps x 2 lanes x 10 ports

**Peak performance (Chip level)**

![Graph showing peak performance](image)

- **A64FX (Fugaku)**: 21.6+ TOPS
- **SPARC64 VIIIfx (K computer)**: 10.8+ TOPS

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Exascale – European Processor Initiative

- EPAC - EPI Accelerator (TITAN)
- MPPA - Multi-Purpose Processing Array
- eFPGA - embedded FPGA
- Cryptographic ASIC (EU Sovereignty)
Arm HPC Software Ecosystem

**Job schedulers and Resource Management:**
- SLURM, IBM LSF, Altair PBS Pro, etc.

**HPC Applications:**
- Open-source, Owned, and Commercial ISV codes

**App/ISA specific optimizations, optimized libs and intrinsics:**
- Arm PL, BLAS, FFTW, etc.

**Parallelism standards:**
- OpenMP (omp / gomp), MPI, SHMEM (see below)

**Programming Languages:**
- Fortran, C, C++
  - via GNU, LLVM, Arm CLA

**Debug and performance analysis tools:**
- Arm Forge, Rogue

**Filesystems:**
- BeeGFS, LUSTRE, ZFS, HDFS, GPFS

**Communication Stacks and run-times:**
- Mellanox IB/OFED/HPC-X, OpenMPI, MPICH, MVAPICH2, OpenSHMEM, OpenUCX, HPE MPI

**Linux OS Distro of choice:**
- RHEL, SUSE, CENTOS, ...

**Arm Server Ready Platform:**
- Standard OS compatible FW and RAS features

**User-space utilities, scripting, containers, and other packages:**
- Singularity, Openstack, OpenHPC, Python, NumPy, SciPy, etc.
Porting HPC apps to the Arm platforms

- GROMACS
- LAMMPS
- CESM2
- MrBayes
- Bowtie
- NAMD
- AMBER
- Paraview
- SIESTA
- UM
- WRF
- Quantum ESPRESSO
- VASP
- MILC
- GEANT4
- OpenFOAM
- GAMESS
- VisIIT
- DL-Poly
- NEMO
- BLAST
- NWCHEM
- Abinit
- BWA
- QMCPACK

Build recipes online at https://gitlab.com/arm-hpc/packages/wikis/home
Arm in IoT

We design & license IP, we do not manufacture chips
Partners build products for their target markets
One size does not fit for all
HPC is a great fit for co-design and collaboration

21 billion chips in the past year
Mobile/Embedded/IoT/Automotive/GPUs
And now ... servers

Arm Technology Connects the World
The New Architecture
HPC is an Architecture

• Historically strong focus on high-end systems and balance:
  • B:F Ratio’s of the late 1990’s thru 2010
  • Parallel processing at massive scale
  • Low-latency / high BW interconnects
  • Citing: S/W maintenance, roll-out, cooling/power

• Workloads:
  • Historical workloads scientific simulation
  • Recent new workloads attracted to “high-end” capabilities of HPC architectures: big data, Deep Learning/AI
  • HPC Leads in technology acceptance (think Formula-1)
  • HPC is an excellent partner for the ecosystem
Arm is Data driven, from the edge to the core
The Cloud to Edge Infrastructure Foundation for a World of 1T Intelligent Devices

Thank You

Arm.com/hpc
Arm’s business model (HPC focus)

**Arm IP**
Armv8.x and extensions, Neoverse IP roadmap SVE Scalable Vector Extension

**Si Partners**
Marvell, Cavium, Fujitsu, Ampere, A64FX

**Platforms**
Hewlett Packard Enterprise, Atos Bull, Sandia National Laboratories, University of Bristol

**Deployment**
Cray, The Supercomputer Company, CEA, EPCC

Software ecosystem
The Future of Arm in HPC

- Scalable Vector Extension Set (SVE)
- Hewlett Packard Enterprise
- TOP 500
- Scalable Vector Extensions
- Arm HPC
- Scalable Vector Extension Set (SVE)