THE EUROPEAN APPROACH FOR EXASCALE AGES

THE ROAD TOWARD SOVEREIGNTY

Jean-marc.denis@European-processor-initiative.eu
Chairman of the Board

THIS PROJECT HAS RECEIVED FUNDING FROM THE EUROPEAN UNION’S HORIZON 2020 RESEARCH AND INNOVATION PROGRAM UNDER GRANT AGREEMENT NO 826647
European Commission President
Jean-Claude Juncker
« Our ambition is for Europe to become one of the top 3 world leaders in high-performance computing by 2020 »
Paris, 27 October 2015

Vice President
Andrus Ansip
« I encourage even more EU countries to engage in this ambitious endeavour »
Digital Day Rome, 23 March 2017

Ministers from seven MS (France, Germany, Italy, Luxembourg, Netherlands, Portugal and Spain) sign a declaration to support the next generation of computing and data infrastructures
The President of the European Union has set new ambitions.

The President of the European Union has set new ambitions. September 16th, 2020.

NextGenerationEU is also a unique opportunity to develop a more coherent European approach to connectivity and digital infrastructure deployment.

None of this is an end in itself - it is about Europe’s digital sovereignty, on a small and large scale.

In this spirit, I am pleased to announce an investment of 8 billion euros in the next generation of supercomputers - cutting-edge technology made in Europe.

And we want the European industry to develop our own next-generation microprocessor that will allow us to use the increasing data volumes energy-efficient and securely.

This is what Europe’s Digital Decade is all about!

EPI OBJECTIVES

- Overall: Develop a complete EU designed high-end microprocessor, addressing Supercomputing and edge-HPC segments

- Short-term objective
  - supply the EU-designed microprocessor to empower the EU Exascale machines

- Long-term objective
  - Europe needs a sovereign (=not at risk of limitation or embargo by non-EU countries) access to high-performance, low-power microprocessors, from IP to products
  - EPI has been set to fulfil this objective
  - EPI has to cover all Technical Readiness levels (TRL)
    - TRL 1-3 are for long-term objectives (EU IP)
    - TRL 4-9 are for short to mid-term objectives (decade) with products designed in EU
FROM OBJECTIVES TO ROADMAP, FROM ROADMAP TO PRODUCTS


**arm**

Short term objective

- TRL ≥6

**RISC-V**

Mid term objective

- TRL <4

General purpose processor (Gen1)

- ARM ZEUS Core

Common Platform

- EPAC IP development & Test chip (22nm)

7nm

GA

EuroHPC ExaScale machines

GPP (Gen2)- ARM >ZEUS Core

EPAC based Accelerator
27 PARTNERS FROM 10 EU COUNTRIES
**FROM IPR TO PRODUCTS**

**FROM EPI TO SIPEARL**

- SIPEARL is
  - Incorporated in EU (France)
  - the industrial and business ‘hand’ of EPI
  - the Fabless company
- licence of IPs from the partners
- develop own IPs around it
- licence the missing components from the market
- Raise in equity the missing budget (~100M€)
- generate revenue from both the HPC, IA, server and eHPC markets
- integrate, market, support & sell the chip
- work on the next generations

Copyright © European Processor Initiative 2020.
HPC & AI AT EXASCALE: IT’S ALL ABOUT WORKFLOWS AND HYBRID SOLUTIONS

- European approach

- ARM IoT Ecosystem

- Edge Computing

- Realtime data processing

- Public Clouds

- Unified environment: Compilers / programming languages / libraries

- EU Architecture

- EU HW

- EU SW

- Handle all complexity in a unified environment

Copyright © European Processor Initiative 2020.
CONSEQUENCES

General Purpose Processors have to be more open

The race to FLOPS is now in the accelerators area
GPP ARCHITECTURE CONCEPT

- ARM-ZEUS GPP core
- EPAC - EPI Accelerator (TITAN)
- MPPA - Multi-Purpose Processing Array
- eFPGA or FPGA - embedded FPGA
- Cryptographic ASIC (EU Sovereignty)
PERSPECTIVES AND CHALLENGES
BY 2022–23, EPI DELIVERS!

- The expertise for developing high-end and complex processing units in Europe, after decades of dis-investment

- A General Purpose Processor for HPC machines can be developed in EU by a EU Company (SiPearl)

- We’ll be ready to move to the next step: engage on the development on a general purpose processor.
CHALLENGES?
DATAFLOW

UNIQUE ARM/NVIDIA COMBINATION FROM DATA CREATION UP TO DATACENTER AND CLOUD?

- Edge Computing
- Realtime data processing

European approach

Unified environment: Compilers / programming languages / libraries

CPU ARM

ACC. A

CPU ARM

RHEA (ARM)

ACC. B

CPU ARM

RHEA + ACC

ACC. C

CPU ARM

RHEA + GPU

ACC. D

CPU ARM

RHEA + GPU

(ARM + Common Platform)

ACC. E

- EU Architecture
- EU HW
- EU SW
- Handle all complexity

Copyright © European Processor Initiative 2020.
THANK YOU FOR YOUR ATTENTION