SoC support in the kernel

Arnd Bergmann <arnd@linaro.org>
Platform/Kernel lifecycle

- Full upstream support
- Updates to new stable kernels
- Fixed kernel version, updates include LTS fixes
- Only vendor updates
- No more kernel updates, machine still running
Platform/Kernel lifecycle

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Obstacles to upstreaming

- GPU drivers
- Android patches
- Short time to market
- Short lifespan
- Unannounced products
- Missing subsystem abstractions
- Competing subsystem abstractions
CPU architectures world map, ca. 2010

Little-Endian
- x86
- Arm
- IA64
- Tile
- SuperH
- MIPS

Big-Endian
- IBM Z
- SPARC
- Power
- PA-RISC
- Microblaze
- OpenRISC
- AVR32
- H8/300
- fr-v
- m68000
- m32r

Endianness
- Big-Endian
- Little-Endian

Categories
- Datacenter
- Server
- Infrastructure
- Industrial
- Embedded
- FPGA, DSP
- Microcontroller
CPU architectures world map, ca. 2010

Little-Endian

Arm
SuperH
MIPS
Xtensa
Microblaze
SoC

Big-Endian

IA64
Alpha
PA-RISC
SPARC
IBM Z

x86

Datacenter
Server
Infrastructure
Industrial
Embedded
FPGA, DSP
Microcontroller
## SoC generations (approximation)

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External SDRAM technologies

Price per Gigabyte

- SDRAM
- M-SDRAM
- DDR
- LP-DDR1
- DDR2
- LP-DDR2
- DDR3
- LP-DDR3
- DDR4
- LP-DDR4(X)
External SDRAM technologies

64 MB DDR $1.82
Armv5/v6, MIPS32
Single-core
External SDRAM technologies

- 64 MB DDR $1.82
  - Armv5/v6, MIPS32
  - Single-core

- 128 MB DDR2 $1.99
  - Armv5/v6/v7, MIPS32
  - Single-core
External SDRAM technologies

- 128 MB DDR2 $1.99
  - Armv5/v6/v7, MIPS32
  - Single-core

- 64 MB DDR $1.82
  - Armv5/v6, MIPS32
  - Single-core

- 512 MB DDR3 $4.17
  - Armv7
dual/quad-core

- Price per Gigabyte
External SDRAM technologies

- 128 MB DDR2 $1.99
  Armv5/v6/v7, MIPS32
  Single-core

- 64 MB DDR $1.82
  Armv5/v6, MIPS32
  Single-core

- 512 MB DDR3 $4.17
  Armv7
  dual/quad-core

- 4 GB LP-DDR4 $44.15
  Armv8, x86
  4+-core
Minimum memory requirements

- Debian 10, 32-bit "armel" port: 256 MB

3.4 Meeting Minimum Hardware Requirements

Once you have gathered information about your computer’s hardware, check that your hardware will let you do the type of installation that you want to do.

Depending on your needs, you might manage with less than some of the recommended hardware listed in the table below. However, most users risk being frustrated if they ignore these suggestions.

Table 3.2 Recommended Minimum System Requirements

<table>
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<tr>
<th>Install Type</th>
<th>RAM (minimum)</th>
<th>RAM (recommended)</th>
<th>Hard Drive</th>
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<tr>
<td>No desktop</td>
<td>256 megabytes</td>
<td>512 megabytes</td>
<td>2 gigabytes</td>
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<td>With Desktop</td>
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Minimum memory requirements

- Debian 10, 32-bit “armel” port: 256 MB
- OpenWRT: 64 MB

**Supportability issues**

It is getting harder or even impossible over time to support devices with low Flash + RAM. **OpenWrt support for those devices will end with the 19.07 release**, i.e. 19.07 will be the last release with support for 4/32 MB devices. There will be no future releases and no images ready for download after 19.07.

**Advice**

Users that are not expert users of OpenWrt (those that can build their own images) should consider

**16/64 as an absolute minimum for any device, with at least 128 MB of RAM being preferred.**

Users should expect that devices with less than 16 MB of flash and/or 64 MB of RAM may be unstable in basic operation under current versions of OpenWrt (17.X, 18.X). They should further expect that support for the device may be dropped at any time and that security patches/updates to the kernel, drivers, and/or application software will
Minimum memory requirements

- Debian 10, 32-bit “armel” port: 256 MB
- OpenWRT: 128 MB
- Alpine Linux: 100 MB

Requirements for Alpine

- A machine to install onto: Alpine supports phones, laptops, desktops, embedded, Raspberries Pi, etc.
  - Most architecture, such as i386, amd64, arm, ppc, and x390.
  - At least 100 MB of RAM is necessary. A complete desktop system can require up to 512 MB.
  - For "sys" or "data" modes, a storage device is needed.
Minimum memory requirements

- Debian 10, 32-bit “armel” port: 256 MB
- OpenWRT: 128 MB
- Alpine Linux: 100 MB
- Sonos legacy products: 8MB (Linux-2.4/2.6, MIPS/PowerPC32/SuperH)

Beginning in May, software updates and new features from Sonos will only be delivered to systems with only modern products.

After May, systems that include legacy products will continue to work as before - but they will no longer receive software updates or new features.

Sonos will work to maintain the existing experience and conduct bug fixes, but our efforts will ultimately be limited by the lack of memory and processing power of these legacy products.
Minimum memory requirements

- Debian 10, 32-bit “armel” port: 256 MB
- OpenWRT: 128 MB
- Alpine Linux: 100 MB
- Sonos legacy products: 8MB (Linux-2.4/2.6, MIPS/PowerPC32/SuperH)
- Microsoft Azure Sphere: 4MB (Linux-5.x, ARMv7-A)

Integrated RAM and flash

Azure Sphere MCUs include a minimum of 4MB of integrated RAM and 16MB of integrated flash memory.

Software architecture and OS
## SoC generations (approximation)

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Low end Linux – race to the bottom

Common features

- Under $5/chip
- Under $10/board
- Diverse CPU architectures
- Small in package RAM
- Low-speed I/O
- Some without MMU
- RTOS competition

Examples

- Broadcom BCM2835 (Armv6K)
- Microchip SAM9X60 (Armv5)
- Mediatek MT7688 (MIPS32)
- ST STM32F4 (Armv7-M)
- Espressif ESP32 (Xtensa)
- Kendryte K210 (RV64)
- Nationalchip GX6605S (C-SKY)
- Ingenic X1000 (MIPS32)
Embedded 32-bit Linux – middle class squeeze

Common features

- Dual/Quad Cortex-A9/A7
- 512/1024MB DDR3
- Larger systems move to 64 bit
- Smaller systems obsolete

Phasing out

- Armv5/v6, MIPS, PowerPC, ...
- Cortex-A15/A17
- USB-3.0/PCIe
- DDR2, LP-DDR2/3/4

Examples

- NXP i.MX6
- Allwinner H3
- Mediatek MT6580
- Xilinx Zynq 7000
- ST STM32MP1
- Qualcomm IPQ4029
- Aspeed AST2600
- Marvell Armada 38x
- TI AM3 (Cortex-A8)
- TI AM5 (Cortex-A15)
- Mediatek MT7621A (MIPS32)
64-bit embedded – taking over

Common features

● Cortex-A53, A72
● Large LP-DDR4
● High-speed I/O

Alternatives

● Embedded x86_64-bit
● Future: RISC-V 64-bit

Examples

● NXP Layerscape, i.MX8
● Renesas R-Car
● Qualcomm Snapdragon
● Rockchip RK33xx
● Amlogic Meson
● Nvidia Tegra
● Mediatek Helio
● Hisilicon Kirin
● Allwinner H-series
● Marvell Armada
● Samsung Exynos
● Xilinx ZynqMP
● ...
Upstream machines in Linux-5.6

- arc: 15 dts files, 15 board files
- arm: 1221 dts files, 242 board files
- arm64: 323 dts files
- c6x: 5 dts files
- csky: 0 dts files, 3 board files
- h8300: 54 dts files, 37 board files
- m68k: 52 dts files, 1 board file
- microblaze: 1 dts file, 1 board file
- mips: 1 dts file
- nds32: 2 dts files, 2 board files
- nios2: 2 dts files
- openrisc: 1 dts file
- powerpc: 200 dts files, 1 board file
- riscv: 1 dts file, 42 board files
- sh: 4 board files
- unicore32: 1 dts file
- x86: 1 dts file
- xtensa: 3 board files
Code size and supported machines

- # Legacy machines
- # DT machines (32 bit)
- # DT machines (64 bit)
- kloc dts
Obsoleted architecture removal

Reasons

- No upstream users
- Migrated to Armv7/v8 cores
- Afterlife as microcontroller/RTOS

Removed in 2018

- Analog Blackfin
- Axis ETRAX CRIS
- Fujitsu FR-V
- Imagination Meta
- Matsushita mn10300
- Mitsubishi m32r
- Sunplus S+Core
- Tilera TileGX
Obsolete architecture removal

Little-Endian

IA64
Tile
x86

Arm

SuperH

Big-Endian

MIPS

Microblaze

IBM Z

Power

SPARC

PA-RISC

Datacenter
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Obsolete architecture removal

Little-Endian

- x86
- Arm
- SuperH
- unicore32

Big-Endian

- IA64
- SPARC
- Power
- IBM Z
- Microblaze
- m68000
- OpenRISC
- h8/300

Endian types:
- Big-Endian
- Little-Endian

Processors:
- Big-Endian:
  - IBM Z
  - SPARC
  - Power
- Little-Endian:
  - x86
  - Arm
  - SuperH
  - unicore32

Embedded:
- Microblaze
- OpenRISC
- h8/300

FPGA, DSP:
- m68000

Industrial:
- SuperH

Server:
- IA64

Datacenter:
- SPARC
- IBM Z

Microcontroller:
- unicore32

Operating Systems:
- Big-Endian: SPARC, IBM Z
- Little-Endian: x86, Arm, SuperH

Endianness concepts:
- Big-Endian: Big-Endian indicates that the most significant byte is stored first in memory.
- Little-Endian: Little-Endian indicates that the least significant byte is stored first in memory.

Arithmetic:
- Big-Endian: Big-Endian arithmetic refers to the way in which binary numbers are processed in computer systems. Big-Endian systems store the high-order bits (most significant bits) of a number in the lowest memory address and the low-order bits (least significant bits) in the highest memory address.
- Little-Endian: Little-Endian arithmetic is the opposite of Big-Endian, where low-order bits are stored in the lowest memory address and high-order bits in the highest memory address.

Example:
- If you have a 32-bit integer 0x12345678, in Big-Endian format, it would be stored as 0x78 0x56 0x34 0x12. In Little-Endian format, it would be stored as 0x12 0x34 0x56 0x78.
2017: Endgame

- Intel Itanium “Kittson”
- Oracle Sparc M8
- Fujitsu SPARC64 XII
- MIPS I6400-F Core
- Andes N15/D15 (nds32)
- Xtensa LX7
- C*Core C9000 (PowerPC32)
User migration

Datacenter

Server

Infrastructure

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FPGA, DSP

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m68000

OpenRISC

h8/300
User migration
## Architectures with new hardware in 2019+

### Obviously

- x86-64
- Armv7-A
- Armv8-A

### Others

- RISC-V (>50 microarchitectures)
- IBM Power 10
- IBM z15
- Synopsys ARC EV7x, VPX5
- Cobham Gaisler Leon5 (SPARC32)
- Xilinx Microblaze 11 (32/64 bit)
- Loongson 3A4000 (mips64)
- Ingenic X1830 (mips32)
- Microchip SAM9x60 (Armv5)
Big-Endian phasing out

- Changing to little-endian
  - PowerPC64
  - Microblaze
  - Realtek MIPS

- MIPS32 Changing to Arm/x86
  - Atheros
  - Broadcom
  - Lantiq

- No new chips after 2017
  - PowerPC32 (NXP, AMCC)
  - SPARC64
  - m68k
  - PA-RISC
  - h8/300

- Started migration to 64-bit RISC-V
  - SPARC32/Leon
  - OpenRISC

- Remaining
  - IBM Z
Endianess change

Little-Endian

x86
Arm
unicore32

Big-Endian

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Little-Endian
New architectures

- **RISC-V (RV32, RV64)**
  - Dozens of cores
  - High expectations
  - No products in 2019

- **Synopsys ARC**
  - 32-bit licensable RISC
  - Active ecosystem
  - Highly popular
  - Limited mainline Linux board support

- **Alibaba C-Sky, Andes NDS32**
  - 32-bit licensable RISC
  - obsoleted by RISC-V

- **Altera/Intel NIOS-II**
  - 32-bit licensable RISC

- **Imagination Meta**
  - Replaced by MIPS, then RISC-V
  - Already gone

- **TI C6x, Qualcomm Hexagon**
  - Proprietary DSPs
  - Linux uncommon
New architectures

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Changesets by architecture and version

- arm
- arm64
- x86
- mips
- powerpc
- s390
- riscv
- ia64
- m68k
- parisc
- sparc
- 23 more
Changesets in minor architectures

RISC-V (riscv)
IA-64 (ia64)
M68K (m68k)
PARISC (parisc)
SPARC (sparc)
ALPHA (alpha)
ND32 (nds32)
CSKY (csky)
MICROBLAZE (microblaze)
SH (sh)
17 more
CPU architectures world map, ca 2020

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Arnd’s prediction for 2030

- x86-64, Armv8+, riscv64 split the market
- Upstreaming further improving
- Last Armv7/RV32 chips released, still shipping
- More creative multi-chip packages
  - Chiplets
  - System-in-package
- IBM Z mainframes still profitable
- No important new ISAs
- Start of 128 bit computing
  - see also CHERI/Morello talk LTD20-110
- Everything else obsolete
Thank you

Accelerating deployment in the Arm Ecosystem
SoC support in the kernel
Arnd Bergmann <arnd@arndb.de>