Linaro Tech Days
LTD20-100K A64FX™:
Power efficient design for HPC and AI

March 24th 2020
Takekazu TABATA
FUJITSU LIMITED
Table of contents

- Introduction
  - Fujitsu processor development history
  - A64FX processor
  - Supercomputer system with A64FX

- Power efficient design for HPC and AI
  - ISA (Collaboration with Arm)
  - Microarchitecture (Collaboration with Riken)
  - A64FX design details

- Software development

- Conclusion
A64FX is the new Fujitsu-designed Arm processor
- It is used in Supercomputer Fugaku, Fujitsu PRIMEHPC FX1000/FX700, and Cray CS500

A64FX is the first processor of the Armv8-A and SVE architecture
- Fujitsu, as a lead partner, collaborated closely with Arm on the development of SVE

A64FX achieves high performance and high power-efficiency in HPC and AI applications
- Fujitsu and Riken tightly collaborate in analyzing and tuning these applications
- Our own microarchitecture maximizes the capability of SVE
- Fujitsu continuously contribute to Arm ecosystem with Linaro
DNA of Fujitsu Processors

- A64FX inherits DNA from Fujitsu technologies used in mainframes, UNIX and HPC servers

  - High reliability
    - Stability
    - Integrity
    - Continuity

  - High speed & flexibility
    - Thread performance
    - Software on Chip
    - Large SMP

  - High performance-per-watt
    - Execution and memory throughput
    - Low power
    - Massively parallel

- CPU w/ extremely high throughput
  - High performance
  - Massively parallel
  - Low power
  - Stability and integrity

Fujitsu’s own microarchitecture design
A64FX Specification

**Architecture Features**
- Armv8.2-A (AArch64 only)
- SVE 512-bit wide SIMD
- 48 computing cores + 4 assistant cores
- Up to 2.2GHz
- HBM2 32GiB
- TofuD 6D Mesh/Torus 28Gbps x 2 lanes x 10 ports
- PCIe Gen3 16 lanes

**7nm FinFET**
- 8,786M transistors
- 594 package signal pins

**Peak Performance (Efficiency)**
- >2.7 TFLOPS (>90%@DGEMM)
- Memory B/W 1024GB/s (>80%@Stream Triad)
Fugaku as the successor of the K computer

The K computer had been in operation for 7 years and was retired in August 2019

Shipping and installation of “Fugaku” started in the end of 2019
Fujitsu launched two models of PRIMEHPC supercomputers using Fugaku Technology

- A64FX is equipped in both products

**PRIMEHPC FX1000**
Supercomputer optimized for large scale computing

High Performance
A64FX processor
384 nodes/Rack
Tohoku Interconnect
Water Cooling
Fujitsu Soft Stack
for Supercomputing

High Scalability

High Density

**PRIMEHPC FX700**
Supercomputer based on standard technologies

Fugaku’s Technology
Ease to use
Installation

A64FX Processor
8 nodes/2U Rackmount
InfiniBand
Air Cooling
Utilize 1SV and Open-Source Soft Stack

Both products are equipped with the world’s first CPU A64FX adopting Scalable Vector Extension (SVE) which is an extension of the ARMv8-A architecture for supercomputers. Moreover, the A64FX developed by integrating the high-performance, low-power CPU design that Fujitsu has developed to far, provides high performance per watt. The CPU not only achieves a high memory bandwidth by using HBM2, but also can handle high-precision arithmetic and multiply-add, which are important in such technologies as deep learning. In this way, the new supercomputers are expected to expand its use in the field of AI.

By developing and offering the new products, Fujitsu will contribute to solving social issues, accelerating leading-edge research and strengthen corporate competitiveness.

1. Product Features

With the support for the new Tohoku Interconnect D as an interconnect and using open-source software (OSS) for HPC middleware. By adopting an air-cooling system and a chassis that can be mounted in a standard server rack, this model is designed to be easily deployed for customers.
## PRIMEHPC FX1000/FX700 specification

<table>
<thead>
<tr>
<th></th>
<th>FX1000</th>
<th>FX700</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CPU</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Name</td>
<td>A64FX</td>
<td>A64FX</td>
</tr>
<tr>
<td>ISA</td>
<td>Armv8.2-A SVE</td>
<td>Armv8.2-A SVE</td>
</tr>
<tr>
<td>Cores</td>
<td>48 computation cores + 2-4 assistant cores</td>
<td>48 computation cores</td>
</tr>
<tr>
<td>Frequency</td>
<td>2.2 GHz</td>
<td>2.0 GHz / 1.8 GHz</td>
</tr>
<tr>
<td>Theoretical peak performance</td>
<td>3.3792 TFLOPS</td>
<td>3.072 TFLOPS / 2.7648 TFLOPS</td>
</tr>
<tr>
<td><strong>Node</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CPUs</td>
<td>1 CPU</td>
<td>1 CPU</td>
</tr>
<tr>
<td>Memory capacity</td>
<td>32 GiB (HBM2)</td>
<td>32 GiB (HBM2)</td>
</tr>
<tr>
<td>Memory bandwidth</td>
<td>1,024 GB/s</td>
<td>1,024 GB/s</td>
</tr>
<tr>
<td>Interconnect</td>
<td>Tofu Interconnect D</td>
<td>InfiniBand EDR</td>
</tr>
<tr>
<td><strong>Enclosure</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Form factor</td>
<td>Dedicated rack</td>
<td>2U rack-mountable chassis</td>
</tr>
<tr>
<td>Node per rack or chassis</td>
<td>384 node/rack</td>
<td>8 node/chassis</td>
</tr>
<tr>
<td>Cooling method</td>
<td>Water cooling</td>
<td>Air cooling</td>
</tr>
</tbody>
</table>

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Fujitsu and Cray announced a partnership

Cray will ship A64FX processor on CS500 supercomputer architecture

Press releases

CRAY AND FUJITSU PARTNER TO POWER SUPERCOMPUTING IN THE EXASCALE ERA

Companies to bring first high-bandwidth memory Arm processor to market

Cray Inc. (a Hewlett Packard Enterprise Company) Limited

SEATTLE and TOKYO, November 13, 2019

Global supercomputer leader Cray, a Hewlett Packard Enterprise company (NYSE: HPE), and leading Japanese information and communication technology company Fujitsu (TSE: 6702), today announced a partnership to offer high-performance technologies for the exascale era. Under the alliance agreement, Cray is developing the first-ever commercial supercomputer powered by the Fujitsu A64FX Arm®-based processor with high-memory bandwidth (HBM) and supported on the proven Cray CS500 supercomputer architecture and programming environment. Initial customers include Los Alamos National Laboratory, Oak Ridge National Laboratory, RIKEN Center for Computational Science, Stony Brook University, and University of Bristol. As part of this new partnership, Cray and Fujitsu will explore engineering collaboration, co-development, and joint go-to-market in an effort to meet customer demand in the supercomputing space.

“Our partnership with Fujitsu means customers now have a broader choice of processor technology to address their pressing computational needs,” said Fred Kohout, senior vice president and CMO at Cray, a Hewlett Packard Enterprise company. “We are delivering the development-to-deployment experience that customers have come to expect from Cray, including exploratory development to the Cray Programming Environment (CPE) for Arm processors to optimize performance and scalability with additional support for Scalable Vector Extensions and high bandwidth memory.”

Cray customers are leaders in their respective fields and often look for opportunities to gain the next edge in performance. The new Fujitsu processor is unique in that it is the first processor to deliver HBM and Arm Scalable Vector Extensions (SVE). HBM2 provides transfer speeds that are significantly faster than DDR4—giving the A64FX a maximum theoretical memory bandwidth greater than 1 terabyte per second (Tb/s), and support for Arm SVE provides improved performance for artificial intelligence and analytics. The Cray CS500 system can apply this compute power to a wide range of HPC and AI workloads while still delivering hallmark features of Arm-based systems with high parallelization, low power consumption and high reliability.

Companies to bring first high-bandwidth memory Arm processor to market

SEATTLE and TOKYO, Nov. 12, 2019 (GLOBE NEWSWIRE) — Global supercomputer leader Cray, a Hewlett Packard Enterprise company (NYSE: HPE), and leading Japanese information and communication technology company Fujitsu (TSE: 6702), today announced a partnership to offer high performance technologies for the Exascale Era. Under the alliance agreement, Cray is developing the first-ever commercial supercomputer powered by the Fujitsu A64FX Arm®-based processor with high-memory bandwidth (HBM) and supported on the proven Cray CS500 supercomputer architecture and programming environment. Initial customers include Los Alamos National Laboratory, Oak Ridge National Laboratory, RIKEN Center for Computational Science, Stony Brook University, and University of Bristol. As part of this new partnership, Cray and Fujitsu will explore engineering collaboration, co-development, and joint go-to-market to meet customer demand in the supercomputing space.
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- Conclusion
A64FX prototype ranked 1st in Green500 list Nov. 2019

- A64FX prototype won #1 on Green500, Nov. 2019
- Cores: 36,864
- Rmax: 1,999.5 [Tflops/s]
- Power Efficacy: 16.876 [GFlops/watts]
- Power: 118 [kW]
- Power quality level 2

By far the best among general purpose CPU only systems:
- 3x better power efficiency than 2nd system (#36 in the list)
A64FX prototype ranked 1\textsuperscript{st} in Green500 list Nov. 2019 (Cont.)

Key for good GFlops/watt is \{energy efficient HW\} \times \{high execution efficiency\}

A64FX is designed for energy efficient

- Fujitsu’s proven CPU microarchitecture & 7nm FinFET
- SoC design: TofuD interconnect integrated
- CoWoS: 4x HBM2 for main memory integrated

Superior execution efficiency

- Well tuned math. Libraries for hardware
- Comm. libraries utilizing long Tofu experience
- Rich performance analyzer/monitor for application tuning
ISA (Collaboration with Arm)

- Developed SVE for new generation vector extension
  - As a lead partner, Fujitsu contributed using our HPC experiences
  - 32 scalable vector registers + 16 predicate registers

- First version of SVE focuses on the HPC and AI applications
  - Supports various data types and arithmetic (incl. for AI application)
  - Includes various features which previous Fujitsu processor supported

- VLA(Vector Length Agnostic) mechanism
  - VLA-enabled binary can be executed on different machines which have different vector length without recompile

  Provides the capability for wider range of applications
  Contributes to build the software ECO system
Co-Design with Riken (1/2)

Feedback for the microarchitecture design
Characteristic of the priority applications etc.

Collaborate tightly

Performance estimation
Characteristic of the hardware behavior etc.

To achieve performance goal for 5 categories / 9 priority issues

- Achievement of a society that provides health and longevity
- Disaster prevention and global climate problems
- Energy problems
- Enhancement of industrial competitiveness
- Development of basic science


- Modify the source codes to align the hardware behavior
- Estimate the application performance using the Fujitsu’s performance estimation tools
- Refine the microarchitecture based on the feedback
- Execute and evaluate the detailed performance using software emulator
Co-Design with Riken (2/2)

RIKEN announced predicted performance of 9 target applications:

- More than **100x faster** than K computer for GENESIS and NICAM+LETKF

- Geometric mean of speedup over the K computer in 9 Priority Issues is greater than **37x+**

### Predicted Performance of 9 Target Applications

<table>
<thead>
<tr>
<th>Area</th>
<th>Priority Issue</th>
<th>Performance Speedup over K</th>
<th>Application</th>
<th>Brief description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Health and Life Sciences</td>
<td>1. Innovative computing infrastructure for drug discovery</td>
<td>125x +</td>
<td>GENESIS</td>
<td>MD for proteins</td>
</tr>
<tr>
<td></td>
<td>2. Personalized and preventive medicine using big data</td>
<td>8x +</td>
<td>Genomon</td>
<td>Genome processing (Genome alignment)</td>
</tr>
<tr>
<td>Disaster prevention and Environment</td>
<td>3. Integrated simulation systems induced by earthquake and tsunami</td>
<td>45x +</td>
<td>GAMERA</td>
<td>Earthquake simulator (FEM in unstructured &amp; structured grid)</td>
</tr>
<tr>
<td>Energy issue</td>
<td>4. Meteorological and global environmental prediction using big data</td>
<td>120x +</td>
<td>NICAM+LETKF</td>
<td>Weather prediction system using big data (structured grid stencil &amp; ensemble Kalman filter)</td>
</tr>
<tr>
<td>Industrial competitiveness</td>
<td>5. New technologies for energy creation, conversion / storage, and use</td>
<td>40x +</td>
<td>NTChem</td>
<td>Molecular electronic simulation (structure calculation)</td>
</tr>
<tr>
<td>Basic science</td>
<td>6. Accelerated development of innovative clean energy systems</td>
<td>35x +</td>
<td>Adventure</td>
<td>Computational Mechanics System for Large Scale Analysis and Design (unstructured grid)</td>
</tr>
<tr>
<td></td>
<td>7. Creation of new functional devices and high-performance materials</td>
<td>30x +</td>
<td>RSDFT</td>
<td>Ab-initio simulation (density functional theory)</td>
</tr>
<tr>
<td></td>
<td>8. Development of innovative design and production processes</td>
<td>25x +</td>
<td>FFB</td>
<td>Large Eddy Simulation (unstructured grid)</td>
</tr>
<tr>
<td></td>
<td>9. Elucidation of the fundamental laws and evolution of the universe</td>
<td>25x +</td>
<td>LGCD</td>
<td>Lattice QCD simulation (structured grid Monte Carlo)</td>
</tr>
</tbody>
</table>

https://postk-web.r-ccs.riken.jp/perf.html
Core microarchitecture design

- **Highly effective performance**
  - 2x 512-bit wide SIMD FMA + Predicate Operation + 4x ALU (shared w/ 2x AGEN)
  - 2x 512-bit wide SIMD load or 512-bit wide SIMD store

- **Good power consumption**
  - Register access reduction mechanism / Fine-grained clock gating technique
Many-Core Architecture design

- **A64FX consists of four CMGs (Core Memory Group)**
  - A CMG consists of 13 cores, an L2 cache and a memory controller
    - One out of 13 cores is an assistant core which handles daemon, I/O, etc.
  - Four CMGs keep cache coherency by ccNUMA with on-chip directory
  - X-bar connection in a CMG maximizes L2 cache throughput
  - Process binding in a CMG allows linear scalability up to 48 cores

- **On-chip-network with a wide ring bus secures I/O performance**
High Bandwidth

Extremely high bandwidth between caches and memory

- A64FX has out-of-order mechanisms in cores, caches and memory controllers. It maximizes the capability of each layer’s bandwidth.
Power efficient design for HPC and AI

Generally, high performance and low power is not easy to achieve at the same time.

A64FX achieves GPU class performance / watt even as a general HPC processor to get over the difficulty.

## Conflicting Demands

### High Performance
- High Bandwidth
- More transistors
- Rich controls
- Many execution units/cache
- Higher Frequency
- More bus width

### Low Power
- Less Transistors
- Less control logic
- Fewer execution units/cache
- Lower Frequency
- Less bus width
Design solution to improve power efficiency

Solution
Unification of logic and physical/power design
• Front-end design always considering design goal (physical design, power design)
• Improved design flow to realize quick feedback between front-end and back-end/custom engineers

Front-end Design
Specrification
Logic design

Back-end Design
Physical Design
Power Estimation

- Register access reduction methodology
- Optimize out-of-order resources for workloads
- Fine-grained clock gating
- Optimized custom cells
- Optimizing buffering and gate sizing and routing optimization
- Timing and power improvements
Unification of logic and physical/power design

ASIC Design Methodology

**Logic Design**
- Hand-off
- Feedback
- P&R, Power Evaluation

**Physical Design**
- P&R, Power Evaluation

Separated Designs makes unnecessary design margins and worse PPA

Unified Design Methodology

**Logic Design**
- Specification design considering power consumption
- Feedback every day and optimize PPA

**Physical Design**
- P&R, Power Evaluation

Logic Designers and Physical Designers working together result in minimum design margins and better PPA

PPA: Performance Power Area

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The performance on 1node is evaluated for seven OSS applications:

- Measured on PRIMEHPC FX1000, A64FX 2.2GHz
- Up to 1.8x faster over latest x86 processor (24 core, 2.9GHz) x2
- High memory B/W and long SIMD length work effectively with these applications

<table>
<thead>
<tr>
<th>Application</th>
<th>Relative Speed Up Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>OpenFOAM</td>
<td>1.5</td>
</tr>
<tr>
<td>FrontISTR</td>
<td>1.0</td>
</tr>
<tr>
<td>ABINIT</td>
<td>0.5</td>
</tr>
<tr>
<td>SALMON</td>
<td>0.5</td>
</tr>
<tr>
<td>SPECFEM3D</td>
<td>1.0</td>
</tr>
<tr>
<td>WRF</td>
<td>1.5</td>
</tr>
<tr>
<td>MPAS</td>
<td>1.5</td>
</tr>
</tbody>
</table>

FUJITSU A64FX        x86 (24core, 2.9GHz)x2
The power efficiency on 1 node is evaluated for seven OSS applications:

- Measured on PRIMEHPC FX1000, A64FX 2.2GHz
- Up to 3.7x more efficient over latest x86 processor (24 core, 2.9GHz) x2
- High power efficiency is achieved by energy-conscious design and implementation

<table>
<thead>
<tr>
<th>Application</th>
<th>Relative Power Efficiency Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>OpenFOAM</td>
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<tr>
<td>FrontISTR</td>
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</tr>
<tr>
<td>ABINIT</td>
<td>3.0</td>
</tr>
<tr>
<td>SALMON</td>
<td>4.0</td>
</tr>
<tr>
<td>SPECFEM3D</td>
<td>2.5</td>
</tr>
<tr>
<td>WRF</td>
<td>3.5</td>
</tr>
<tr>
<td>MPAS</td>
<td>4.0</td>
</tr>
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FUJITSU A64FX vs. x86 (24core, 2.9GHz)x2
Table of contents

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RIKEN and Fujitsu are developing software stacks for the supercomputer Fugaku
- Fujitsu compilers are optimized for the microarchitecture, maximizing SVE and HBM2 performance
- We collaboratively work with RIKEN / Linaro / OpenHPC / OSS communities / ISVs and contribute to Arm HPC ecosystem

Fugaku applications

<table>
<thead>
<tr>
<th>Management software</th>
<th>File system</th>
<th>Programming environment</th>
</tr>
</thead>
<tbody>
<tr>
<td>System management for high availability &amp; power saving operation</td>
<td>FEFS Lustre-based distributed file system</td>
<td>XcalableMP, FDPS</td>
</tr>
<tr>
<td>Job management for higher system utilization &amp; power efficiency</td>
<td>LLIO NVM-based file I/O Accelerator for Fugaku</td>
<td>Open MPI, MPICH(PiP), DTF</td>
</tr>
</tbody>
</table>

Multi-Kernel System: RHEL8 and light-weight kernel (IHK/McKernel)

Fugaku system hardware

- Tensorflow
- Chainer
- Pytorch
- Docker
- KVM
- Singularity

FDPS: Framework for Developing Particle Simulator
PiP: Process-in-Process
DTF: Data Transfer Framework
IHK: Interface for Heterogeneous Kernels
RIKEN and Fujitsu verify Spack’s 3000+ recipes with multiple compilers

- Spack is a Flexible Package Manager for HPC Software
- The verification results are available on the RIKEN’s web page
  https://postk-web.r-ccs.riken.jp/oss/public/

Summary of results
  - Spack version used: October 31, 2019

<table>
<thead>
<tr>
<th></th>
<th>GNU GCC</th>
<th>Clang</th>
<th>Fujitsu Compiler (under development)</th>
</tr>
</thead>
<tbody>
<tr>
<td>x86</td>
<td>2603/3574 (72.83%)</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>aarch64</td>
<td>2546/3574 (71.24%)</td>
<td>1547/3574 (43.28%)</td>
<td>2409/3574 (67.40%)</td>
</tr>
</tbody>
</table>
Software Stacks for AI on Arm

AI Software Stack with OSS

- A64FX can execute Arm AI software stack
- Fujitsu is porting and tuning DNNL for A64FX/SVE
- We continue to contribute through porting and tuning AI software stack
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Conclusion

- A64FX is integrated Fujitsu’s proven microarchitecture with Arm ISA and feedbacks from co-design.
- A64FX is the first processor of the Armv8-A SVE architecture.
  - It is used for supercomputer Fugaku, Fujitsu PRIMEHPC and Cray CS500.
- A64FX achieves high performance and high performance/watt in HPC and AI areas.
- Fujitsu collaboratively works with partners and continuously contributes to Arm ecosystem and Arm software stacks with Linaro.