Open Source Heterogeneous SW Stacks
For Embedded Devices

Tomas Evensen
CTO, Embedded Software
4/4/2019
The Future in Heterogenous SoCs

Versal ACAP

- Scalar Processing Engines
- Adaptable Hardware Engines
- Intelligent Engines
  SW Programmable, HW Adaptable
- Breakout Integration of Advanced Protocol Engines
FPGA: The “Chameleon” Chip

FPGA includes:
- Programmable logic (LUTs)
- Hardened DSP blocks
- Hardened memory (BRAM, URAM)

FPGAs are programmed with:
- Preoptimized libraries
- VHDL, Verilog
- High-level synthesis (HLS, C to gates)

FPGAs are great to implement:
- Parallel compute (e.g. MAC)
  - With variable precision
- Parallel, flexible dataflows
  - Build your own buses
- Flexible, multiport memory hierarchies

What is FPGA/Fabric/Programmable Logic:
- Is it glue logic?
- Is it a powerful parallel DSP engine?
- Is it an RTL simulator?

Yes!!! And more…
CPU Architectures not Scaling with Workloads

- Processor frequency scaling ended in 2007
- Multicore architecture scaling has flattened

Workloads require higher performance, lower latency
- Cloud: video, big data, AI...
- Edge: auto, surveillance, AI...

Solution is specialized heterogeneous execution engines
Example of Integration in Industrial Automation

PLC
- High performance Single Core CPU
  - Typically “end user application dependent”
  - Application 1
  - Application 2
  - HMI
  - RTOS
  - OS
  - Single CPU

Drive
- Single Core CPU + Single Core DSP
  - Typically “time critical”
  - Network I/F
  - Motion Control
  - Motor Control
  - RTOS
  - Single CPU
  - Single DSP

Safety Logic
- Two independent Core CPU
  - “safety critical”
  - Safety Application
  - Safety Application
  - Bare Metal
  - Bare Metal
  - Single CPU
  - Single CPU
  - Voter

Integration into Single Hardware Unit
Zynq® UltraScale+™ MPSoC
Execution Environments within Zync US+ MPSoC

- Multiple core clusters
  - A53, R5, MicroBlaze

- Multiple Execution Levels (EL)
  - EL0 – User space – Linux apps, Containers, RTOS apps
  - EL1 – OS space – Linux kernel, RTOS + RTOS apps
  - EL2 – Hypervisor – Xen, Jailhouse, …
  - EL3 – Firmware – ARM Trusted Firmware

- Multiple Security Environments
  - TrustZone (TZ) – HW protecting resources (e.g. memory)
  - Trusted Execution Environment (TEE) – SEL1

- Multiple Operating systems
  - Linux is used in majority of use cases
    - Including Android
  - Most free and commercial RTOS’s are being used
    - FreeRTOS, Zephyr, VxWorks, Integrity, Nucleus, uC/OS, OSE, ThreadX
    - QNX/Neutrino, Sciopla, eT-kernel, Lynx, PikeOS, …
  - Bare metal (no OS) is common on smaller cores
  - OS often pinned to specific core for embedded applications

© Copyright 2019 Xilinx
Can We Simplify SW for Heterogenous Environments?

- Today, most heterogeneous environments are clobbered together ad-hoc
  - Everybody coming up with their own shared memory scheme
- Can we standardize how environments interact?
  - How to configure the environments?
  - How to manage (lifecycle) the environments?
  - How to pass messages between environments?
  - How to share resources between environments?
  - How to port any OS on top of a standardized abstraction layer?
- Can we have an open source implementation solving these problems?
  - Based on already existing open source projects?

These are the questions OpenAMP tries to answer
OpenAMP Initiative

> Asymmetric Multiprocessing (AMP): Mixing multiple OS’s
  ➢ Xilinx heterogeneous systems are at the bleeding edge of AMP
  ➢ Up to now: No standards. Very ad-hoc.

> OpenAMP is an open AMP framework that includes two efforts:
  1. A standardized way of using AMP driven by the Multicore Association*
  2. A clean-room open source implementation/project

> OpenAMP currently includes the following components:
  ➢ Lifecycle operations - Such as start/stop another environment
  ➢ Messaging - Sending and receiving messages
  ➢ Low level abstractions – Sharing memory, inter-processor interrupts, …
  ➢ Proxy operations - Remote access to services, e.g. file system
  ➢ Coming soon: Resource configuration using System Device Trees

> Built on top of existing open source projects/standards
  ➢ RemoteProc, rpmsg, Virtio, Device Trees

> MCA OpenAMP Working Group
  ➢ Currently Xilinx, ST, TI, Mentor, Qualcomm, Wind River, Micrium, Express Logic, Linaro, …

> Accelerate adoption by working in open source
  ➢ Open Linux and RTOS implementations

* New OpenAMP organization under consideration
System Device Tree to Device Trees

- System Device Tree describes the “full” HW with multiple address spaces
- Produces one or more "regular" device trees from a system device tree ("pruning")
- Output are fully compatible device trees
- It supports domain specific configurations, i.e. memory and device assignment
Conceptual Allocation of Applications in Multicore SoC

High Criticality
- App1 - RT Industrial Networking
- App2 – IoT Gateway TSN
- App3 SIL supervisor

Low Criticality
- App4 – Streaming
- App5 – HMI
- App6 – ML

Mid Criticality
- App7 PLC
- App8 Motion

High Criticality
- App9 Motor Control
- App10 Safety Loop

Hypervisor use case
- Similar separation as AMP
- OSes pinned to cores
- OpenAMP for messaging
- System Device Trees for configuration

Issue: L2 cache
- Architected for SMP
- Cache locking not available
- Linux can thrash cache

Potential solution
- Cache coloring

HMI = Human Machine Interface
ML = Machine Learning
TSN = Time Sensitive Network
SIL = Safety Integrity Level
OCM = On Chip Memory
TCM = Tightly Coupled Memory

© Copyright 2019 Xilinx
Cache coloring

> Cache coloring is a software technique for cache partitioning without hardware support
  > Fragments the memory space into a set (colors)
  > Color addresses are mapped to disjoint cache partitions
  > Achieved by dividing the physical memory space into sequential regions

> For example 1G bytes of memory

Size of a sub-region assigned to a colour for example 4K byte
Cache coloring + Hypervisor

High Criticality
App1 - RT Industrial Networking
App2 – IoT Gateway TSN
App3 SIL supervisor

Low Criticality
CPU0
App4 - Streaming
App5 – HMI
App6 – ML
Linux
RTOS
Bare Metal

Mid Criticality
CPU1
Color #2
CPU2
App8 Motion
App7 PLC

High Criticality
Color #3-#4
CPU3
App9 Motor Control
App10 Safety Loop

Hypervisor

Memory Controller

Color #1 #2
External Memory

128K

Color #3 #4

64K

128K

HMI = Human Machine Interface
ML = Machine Learning
TSN = Time Sensitive Network
SIL = Safety Integrity Level
OCM = On Chip Memory
TCM = Tightly Coupled Memory

© Copyright 2019 Xilinx

> Jailhouse Hypervisor
>> SIEMENS Open Source:
https://github.com/siemens/jailhouse

> Study of Cache Coloring
>> Xilinx
>> University of Modena
https://hipert.unimore.it/
>> Evidence
http://www.evidence.eu.com/

> Results
>> Interference amongst Core 3 and Core 2 is eliminated

> Predictability improved

> Separation improved

> Xen implementation next
Try out Heterogenous Compute Yourself

- Ultra96-V2 from AVNET
- $249 Single Board Computer (SBC)
  - Based on Xilinx Zynq UltraScale+
  - Replaces Ultra96
- Designed to 96Boards.org standard form-factor
  - Consumer edition
- Applications
  - Artificial intelligence
  - Machine learning
  - Embedded processing
  - Robotics
Ultra96-V2 Kit Overview

- What’s included
  - Ultra96-V2 board
  - 16 GB microSD card
  - SDSoC license voucher
  - Quick start card
- Part number: AES-ULTRA96-V2-G
- Availability
  - May
- Additional information
  - http://avnet.me/NewUltra96V2
  - http://avnet.me/ultra96-v2
What about Multi-chip Heterogenous Systems

Traditional Accelerator Attach:

SW DMA Engine: Clean and copy data

Processor

CPU

CPU

CPU

CPU

On-chip bus

Memory

OS Virtual Memory

Accelerator

PCle

System Bus

Private Accel Memory
Accelerators are Becoming Smarter

More work being offloaded to accelerators
- ML, video/audio, analytics

Smart Accelerators running software stacks
- Software defined networks and storage

Increased accelerator-accelerator data transfers
- Remote Direct Memory Access (RDMA), security
‘Driverless’ model, it’s all memory

On-chip = multichip

Eliminates bespoke DMA driver

Enables, cache coherent fine grain data sharing

Builds on PCIe standard and infrastructure
The CCIX Consortium

- Incorporated in 2017
- 50 Members & Growing
- Complete Ecosystem
- Join CCIX Now!

Promotors
- AMD
- arm
- Huawei
- Qualcomm
- Xilinx

Contributors
- Arteris, Inc.
- Baikal Electronics
- Bitman Technologies, Inc.
- Chengdu Higon Integrated Circuit Design Co., Ltd.
- Ericsson AB
- Guizhou Huaxintong Semiconductor Technology Co. Ltd.
- INVECAS, Inc.
- Nokia Solutions and Networks Oy
- Parade Technologies, Inc.
- Phytium Technology Co., Ltd.
- PLDA
- Shanghai Zhaoxin Semiconductor Co., Ltd.
- Silicon Laboratories Inc.
- SmartDV Technologies India Private Ltd.
- Socionext Inc.
- Viavi Solutions, Inc.
- Wave Computing

Adopters
- Cadence
- Broadcom
- Cadence
- Marvell
- Micron
- Samsung
- Samtec
- SK hynix
- Synopsys
- Western Digital
Adaptable.
Intelligent.